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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,286	03/24/2004	Tetsuo Kawano	1450.1040	3924

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EXAMINER	
LAM, NELSON C	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,286	KAWANO ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication of 03/24/2004. Application 10/807,286 has been examined. In the examination of 10/807,286, claims 1-15 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 2-8, 10-11 and 13 are objected to because of the following informalities: Claim limitations need to be separated with a semicolon. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-15 are rejected under 35 U.S.C. 102(e)** as being anticipated by Andou (US Patent Application Publication No. US 2004/0254776 A1).

As per **claim 1**, Andou discloses a timing analysis apparatus (Fig. 2; [0106]) for performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a coefficient arithmetically operating unit for calculating variation coefficients of delay time in a target path being an analysis target with a variation in delay time in each gate being cancelled out in accordance with a number of gate stages in the target path in the semiconductor integrated circuit (Abstract; [0035]; [0057]; [0059]); and

a first timing analysis unit for performing timing analysis in the target path based on the calculated variation coefficients and the circuit information ([0091]; Fig. 1, #D15; [0104]).

As per **claim 2**, Andou discloses the timing analysis apparatus according to claim 1,

wherein said coefficient arithmetically operating unit comprises a coefficient of the number of stages arithmetically operating section for calculating coefficients of the number of stages indicating variation amounts in delay time according to the number of gate stages in the target path based on the circuit information ([0057]; [0092]),

a variation width arithmetically operating section for calculating a variation width of delay time in the entire target path based on the circuit information ([0124]), and

a variation coefficient arithmetically operating section for calculating the variation coefficients of the delay time in the target path based on the calculated coefficients of the number of stages and the variation width of the delay time ([0057]; [0092]).

As per **claim 3**, Andou discloses the timing analysis apparatus according to claim 2, further comprising:

a table of coefficients of the number of stages in which an optional number of gate stages in a path and the coefficients of the number of stages are made to correspond to each other (Fig. 2, #26; [0111]; where the database stores a table of coefficients),

wherein said coefficient of the number of stages arithmetically operating unit obtains the coefficients of the number of stages according to the number of gate stages in the target path with reference to said table of the coefficients of the number of stages (Fig. 1, #D15; [0104]).

As per **claim 4**, Andou discloses the timing analysis apparatus according to claim 1, further comprising:

an information input unit for inputting the circuit information therein and extracting delay information relating to delay time of each gate in the target path from the circuit information, wherein said coefficient arithmetically operating unit calculates the variation coefficients of the delay time in the target path based on the extracted delay information of each gate (Fig. 1; [0100]; [0101]; [0102]; [0103]; [0104]; [0105]).

As per **claim 5**, Andou discloses the timing analysis apparatus according to claim 1, wherein said first timing analysis unit verifies whether previously specified timing conditions are satisfied in the target path or not, based on the calculated variation coefficients and the circuit information ([0057]; [0092]).

As per **claim 6**, Andou discloses the timing analysis apparatus according to claim 5, wherein the timing conditions are the conditions relating to setup time and hold time in the target path ([0043]; Fig. 1, #S14; [0105]).

As per **claim 7**, Andou discloses the timing analysis apparatus according to claim 1, further comprising,

a second timing analysis unit for performing timing analysis in the target path by accumulating a variation in the delay time of each gate in the target path, based on the circuit information (Abstract; [0035]; [0057]; [0059]); and

a determination unit for determining whether previously specified timing conditions are satisfied or not based on a result of timing analysis supplied from said second timing analysis unit ([0121]; [0122]; [0123]; [0124]),

wherein said coefficient arithmetically operating unit calculates the variation coefficients of the delay time in the target path only when it is determined that the timing conditions are not satisfied in said determination unit ([0122]).

As per **claim 8**, Andou discloses the timing analysis apparatus according to claim 7, further comprising:

an information input unit for inputting the circuit information therein and extracting delay information relating to the delay time of each gate in the target path (Fig. 1, #D11, D12, D13, S11; [0101]),

wherein said second timing analysis unit performs timing analysis of the target path based on the extracted delay information of each gate ([0104]; [0105]).

As per **claim 9**, Andou discloses a timing analysis method for performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a delay information extracting step of having the circuit information inputted and extracting delay information relating to delay time of each gate in a target path being an analysis target in the semiconductor integrated circuit from the circuit information (Fig. 1; [0100]; [0101]; [0102]; [0103]; [0104]; [0105]);

a coefficient arithmetically operating step of calculating variation coefficients of the delay time in the target path with a variation in the delay time in each gate being cancelled out in accordance with the number of gate stages in the target path based on the delay information extracted in said delay information extracting step (Abstract; [0035]; [0057]; [0059]); and

a first timing analysis step of performing timing analysis in the target path with use of the variation coefficients calculated in said coefficient arithmetically operating step and the circuit information ([0091]; Fig. 1, #D15; [0104]).

As per **claim 10**, Andou discloses the timing analysis method according to claim 9, further comprising:

a second timing analysis step of performing timing analysis in the target path by accumulating the variation in the delay time of each gate in the target path based on the delay information extracted in said delay information extracting step (Abstract; [0035]; [0057]; [0059]); and

a determination step of determining whether previously specified timing conditions are satisfied or not based on an analysis result in said second timing analysis step, wherein said coefficient arithmetically operating step is executed only when it is determined that the timing conditions are not satisfied in said determination step ([0121]; [0122]; [0123]; [0124]).

As per **claim 11**, Andou discloses the timing analysis method according to claim 9,

wherein said coefficient arithmetically operating step comprises a coefficient of a number of stages arithmetically operating step of calculating coefficients of a number of stages showing variation amounts of delay time according to the number of gates in the target path based on the circuit information ([0057]; [0092]);

a variation width arithmetically operating step of calculating a variation width of delay time of the entire target path based on the circuit information ([0124]); and

a variation coefficient arithmetically operating step of calculating the variation coefficients of the delay time in the target path based on the coefficients of the number of stages calculated in said coefficient of the number of stages arithmetically operating step and the variation width of the delay time calculated in said variation width arithmetically operating step ([0057]; [0092]).

As per **claim 12**, Andou discloses a program product for making a computer execute (Fig. 2, #25, #25a; [0109]):

a delay information extracting step of extracting delay information relating to delay time of each gate in a target path being an analysis target in a semiconductor integrated circuit from circuit information of the semiconductor integrated circuit (Fig. 1; [0100]; [0101]; [0102]; [0103]; [0104]; [0105]);

a coefficient arithmetically operating step of calculating variation coefficients of delay time in the target path with a variation in the delay time in the each gate being cancelled out in accordance with a number of gate stages in the target path, based on the delay information extracted in said delay information extracting step (Abstract; [0035]; [0057]; [0059]); and

a first timing analysis step of performing timing analysis in the target path with use of the variation coefficients calculated in said coefficient arithmetically operating step and the circuit information ([0091]; Fig. 1, #D15; [0104]).

As per **claim 13**, Andou discloses the program product according to claim 12 for making the computer execute:

a second timing analysis step of performing timing analysis in the target path by accumulating the variation in the delay time of each gate in the target path based on the delay information extracted in said delay information extracting step (Abstract; [0035]; [0057]; [0059]); and

a determination step of determining whether previously specified timing conditions are satisfied or not based on an analysis result in said second timing analysis step, wherein only when it is determined that the timing conditions are not satisfied in

said determination step, said program product makes the computer execute said coefficient arithmetically operating step ([0121]; [0122]; [0123]; [0124]).

As per **claim 14**, Andou discloses the program product according to claim 12,

wherein said coefficient arithmetically operating step comprises a coefficient of a number of stages arithmetically operating step of calculating coefficients of a number of stages indicating variation amounts of delay time according to the number of gate stages in the target path based on the circuit information ([0057]; [0092]);

a variation width arithmetically operating step of calculating a variation width of delay time in the entire target path based on the circuit information ([0124]); and

a variation coefficient arithmetically operating step of calculating the variation coefficients of the delay time in the target path based on the coefficients of the number of stages calculated in said coefficient of the number of stages arithmetically operating step and the variation width of the delay time calculated in said variation width arithmetically operating step ([0057]; [0092]).

As per **claim 15**, Andou discloses the program product according to claim 14, wherein the coefficients of the number of stages according to the number of gate stages in the target path is obtained with reference to a table of the coefficient of the number of stages with an optional number of gate stages in a path and the coefficient of the number of stages being made correspond to each other, recorded in a recording medium (Fig. 2, #26; [0111]; where the database stores a table of coefficients).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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